In the Claims:

1. (previously presented) An integrated circuit SRAM cell, comprising:

a substrate which includes at least one substantially monolithic body of semiconductor material;

a first patterned thin-film layer comprising polysilicon;

a second patterned thin-film layer comprising polysilicon and overlying said first thin-film layer, said second layer being doped to provide high conductivity;

a patterned interlevel dielectric overlying portions of said first and second thin-film layers, said interlevel dielectric including multiple independently planarized layers of dielectric material therein, said multiple independently planarized layers including a lower portion of a spin-on glass a middle portion of a dielectric material which is not spin-on glass, and an upper portion of spin-on glass;

a third patterned thin-film layer comprising polysilicon having a very high resistivity;

wherein said first patterned thin-film layer is configured to provide transistor gates, and said first and second thin-film layers are interconnected to provide an array of latches, and said third thin-film layer overlies said patterned interlevel dielectric and is interconnected through contact holes with said first and second layers to provide resistive loads for each said latch.

2. (original) The integrated circuit of claim 1, wherein said first thin-film layer also comprises a silicide cladding.

3. (original) The SRAM cell of claim 1, wherein said interlevel dielectric comprises two layers of spin-on glass.

4. (original) The SRAM cell of claim 1, wherein said interlevel dielectric also comprises at least two dielectric layers which are not planarized.

5. (original) The SRAM cell of claim 1, wherein said second interlevel dielectric comprises at least four layers.

6. (original) The SRAM cell of claim 1, wherein said loads each have a resistance value of about 1TΩ.

7. (previously presented) An integrated circuit SRAM cell, comprising:

first and second overlaid thin-film conductor layers, each comprising clad polysilicon, at least one of said conductor layers being capacitively coupled to substantially monolithic semiconductor material to define field-effect transistor channels therein;

a patterned interlevel dielectric overlying portions of said second thin-film layer, and including multiple independently planarized layers of dielectric material therein, said multiple independently planarized layers of dielectric material including at least three different layers of dielectric material, with at least two of said layers of dielectric material being independently planarized layers of spin-on glass;

a third patterned thin-film layer comprising polysilicon having a very high resistivity, and lying on a substantially planar top surface of said patterned interlevel dielectric;

wherein said first and second thin-film layers are interconnected to provide an array of latches, and said third thin-film layer overlies said patterned interlevel dielectric and is interconnected through contact holes with said first and second layers to provide passive loads for respective ones of said latches.

8. (original) The SRAM cell of claim 7, wherein said interlevel dielectric comprises two layers of spin-on glass.

9. (original) The SRAM cell of claim 7, wherein said interlevel dielectric also comprises at least two dielectric layers which are not planarized.

10. (original) The SRAM cell of claim 7, wherein said interlevel dielectric comprises at least four layers.

11. (original) The SRAM cell of claim 7, wherein said loads each have a resistance value of about 1TΩ.

12. (previously presented) An integrated circuit SRAM cell, comprising:

at least one patterned thin-film conductor layer comprising polysilicon and being capacitively coupled to substantially monolithic semiconductor material to define field-effect transistor channels therein;

a patterned interlevel dielectric overlying said at least one patterned thin-film conductor layer, and including multiple independently planarized layers of dielectric materials therein, said multiple independently planarized layers of dielectric material including at least three different layers of dielectric material, with at least two of said layers of dielectric material being independently planarized layers of spin-on glass;

an additional patterned thin-film layer comprising polysilicon, and lying on a substantially planar top surface of said patterned interlevel dielectric;

wherein said at least one patterned thin-film conductor layer is interconnected to provide an array of latches, and said additional thin-film layer overlies said patterned interlevel dielectric and is interconnected through contact holes with said conductor layers to provide passive loads for respective ones of said latches.

13. (original) The SRAM cell of claim 12, wherein said additional layer comprises SIPOS.

14. (original) The SRAM cell of claim 12, wherein said additional layer comprises polysilicon doped with chlorine.

15. (original) The SRAM cell of claim 12, wherein said interlevel dielectric comprises two layers of spin-on glass.

16. (original) The SRAM cell of claim 12, wherein said interval dielectric also comprises at least two dielectric layers which are not planarized.

17. (original) The SRAM cell of claim 12, wherein said interlevel dielectric comprises at least four layers.

18. (original) The SRAM cell of claim 12, wherein said loads each have a resistance value of about 1TΩ.

19. (previously presented) The integrated circuit SRAM cell of claim 1 wherein the third patterned thin-film layer comprises substantially undoped polysilicon.

20. (previously presented) The integrated circuit SRAM cell of claim 19 wherein the substantially undoped polysilicon comprises intrinsic polysilicon.

21. (previously presented) The integrated circuit SRAM cell of claim 1 wherein the third patterned thin-film layer comprises a polysilicon layer doped with chlorine.

22. (previously presented) The integrated circuit SRAM cell of claim 7 wherein the third patterned thin-film layer comprises substantially undoped polysilicon.

23. (previously presented) The integrated circuit SRAM cell of claim 22 wherein the third patterned thin-film layer comprises intrinsic polysilicon.

24. (previously presented) The integrated circuit SRAM cell of claim 7 wherein the third patterned thin-film layer comprises a polysilicon layer doped with chlorine.

25. (previously presented) The integrated circuit SRAM cell of claim 12 wherein the third patterned thin-film layer comprises substantially intrinsic polysilicon.

26. (currently amended) An integrated circuit SRAM cell formed in a semiconductor substrate, a plurality of active transistor regions being formed in the substrate, the SRAM cell comprising:

a first conductive layer disposed on the semiconductor substrate, the first conductive layer forming a plurality of respective control nodes for respective transistors in the substrate;

a second conductive layer disposed over the first conductive layer, the second conductive layer being coupled to the first conductive layer and to active transistor regions to interconnect groups of transistors and thereby form respective data latches;

an interlevel dielectric disposed on the second conductive layer and including three different ~~insulating~~dielectric layers, two of the three dielectric~~insulating~~ layers being ~~separately~~ independently planarized spin-on glass layers;

an insulating layer disposed on the interlevel dielectric; and

a third conductive layer formed on the insulating layer, the third conductive layer being coupled to the data latches to form respective resistive loads for the respective latches.

27. (currently amended) An integrated circuit SRAM cell formed in a semiconductor substrate, a plurality of active transistor regions being formed in the substrate, the SRAM cell comprising:

a first conductive layer disposed on the semiconductor substrate, the first conductive layer forming a plurality of respective control nodes for respective transistors in the substrate;

a second conductive layer disposed over the first conductive layer, the second conductive layer being coupled to the first conductive layer and to active transistor regions to interconnect groups of transistors and thereby form respective data latches;

a plurality of independently~~separately~~ planarized spin-on glass layers disposed on the second conductive layer;

an insulating layer disposed on a top one of the planarizing spin-on glass layers;

a third conductive layer formed on the insulating layer, the third conductive layer being coupled to the data latches to form respective resistive loads for the respective latches; and

wherein the plurality of independently~~separately~~ planarized spin-on glass layers includes a first independently planarized spin-on glass layer disposed on the second conductive layer, an oxide layer disposed on the first spin-on glass layer, and a second independently planarized spin-on glass layer disposed on the oxide layer.

28. (previously presented) The integrated circuit SRAM cell of claim 26 wherein each of the conductive layers comprises a suitably doped polysilicon layer.

29. (previously presented) The integrated circuit SRAM cell of claim 26 wherein the first conductive layer comprises a first polysilicon layer and a cladding layer formed on the first polysilicon layer.

30. (previously presented) The integrated circuit SRAM cell of claim 29 wherein the cladding layer comprises tantalum silicide.

31. (previously presented) The integrated circuit SRAM cell of claim 26 wherein the second conductive layer comprises a second polysilicon layer and a cladding layer formed on the second polysilicon layer.

32. (previously presented) The integrated circuit SRAM cell of claim 31 wherein the cladding layer comprises tantalum silicide.

33. (currently amended) An integrated circuit SRAM cell formed in a semiconductor substrate, a plurality of active transistor regions being formed in the substrate, the SRAM cell comprising:

a first conductive layer disposed on the semiconductor substrate, the first conductive layer forming a plurality of respective control nodes for respective transistors in the substrate;

a second conductive layer disposed over the first conductive layer, the second conductive layer being coupled to the first conductive layer and to active transistor regions to interconnect groups of transistors and thereby form respective data latches;

a plurality of different independently planarized~~planarizing~~ spin-on glass layers disposed on the second conductive layer;

a dielectric layer disposed between two of the independently planarized spin-on glass layers, the dielectric layer being different from the two independently planarized spin-on glass layers;

an undoped oxide layer disposed on a top one of the planarized~~ing~~ spin-on glass layers; and

a third conductive layer formed on the insulating layer, the third conductive layer being coupled to the data latches to form respective resistive loads for the respective latches.

34. (previously presented) The integrated circuit SRAM cell of claim 26 wherein the third conductive layer comprises intrinsic polysilicon.